

PUBLICATION-DATE: February 27, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 709/206; 718/102

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems, methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable, deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Ir
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☐ 3. Document ID: US 20030034885 A1

L19: Entry 3 of 41

File: PGPB

Feb 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030034885

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030034885 A1

TITLE: Medical gas alarm system

PUBLICATION-DATE: February 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Catton, Edward W.	New Palestine	IN	US	
Sharer, John M.	Batesville	IN	US	
Wilker,, John B. SR.	St. Leon	IN	US	
Plyler, Phillip B.	Atlanta	GA	US	
Abel, Joseph H.	New Palestine	IN	US	
Kaht, William J.	Burlington	KY	US	
Hentges, James P.	Fountain City	WI	US	
Pfingsten, Thomas R.	Winona	MN	US	

Breitlow, Stanton H.	Winona	MN	US
Bohlinger, William C.	Buffalo City	WI	US
Dubisar, Thomas J.	Winona	MN	US
Moran, Robert O.	Onanlaska	WI	US
Wolfe, Dale T.	Onalask	WI	US
LaBare, Nick D.	Winona	MN	US
Hoffman, Richard E.	Overland Park	KS	US

US-CL-CURRENT: 340/506; 340/531, 340/611, 340/614

ABSTRACT:

A medical gas alarm system for use in a healthcare facility having a medical gas system and having a network of computer devices is provided. The alarm system includes at least one area alarm controller adapted to receive a first signal indicative of a condition of a first portion of the medical gas system. The area alarm controller is adapted to communicate with the network. The alarm system also includes at least one master alarm controller adapted to receive a second signal indicative of a condition of a second portion of the medical gas system. The master alarm controller is adapted to communicate with the network. The area alarm controller is adapted to communicate with the master alarm controller through the network.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	In
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☐ 4. Document ID: US 20030009694 A1

L19: Entry 4 of 41

File: PGPB

Jan 9, 2003

PGPUB-DOCUMENT-NUMBER: 20030009694

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030009694 A1

TITLE: Hardware architecture, operating system and network transport neutral system, method and computer program product for secure communications and messaging

PUBLICATION-DATE: January 9, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 713/201; 713/151, 713/176

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems,

methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable, deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. Desc	In
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☐ 5. Document ID: US 20020199096 A1

L19: Entry 5 of 41

File: PGPB

Dec 26, 2002

PGPUB-DOCUMENT-NUMBER: 20020199096

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020199096 A1

TITLE: System and method for secure unidirectional messaging

PUBLICATION-DATE: December 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 713/153

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems, methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable, deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. Desc	In
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☐ 6. Document ID: US 20020199001 A1

L19: Entry 6 of 41

File: PGPB

Dec 26, 2002

PGPUB-DOCUMENT-NUMBER: 20020199001
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020199001 A1

TITLE: System and method for conducting a secure response communication session

PUBLICATION-DATE: December 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 709/227; 709/237, 713/200

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems, methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable, deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw Desc	In
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☐ 7. Document ID: US 20020196935 A1

L19: Entry 7 of 41

File: PGPB

Dec 26, 2002

PGPUB-DOCUMENT-NUMBER: 20020196935
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020196935 A1

TITLE: Common security protocol structure and mechanism and system and method for using

PUBLICATION-DATE: December 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 380/37; 380/28

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems, methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable, deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	In
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☐ 8. Document ID: US 20020194501 A1

L19: Entry 8 of 41

File: PGPB

Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020194501
 PGPUB-FILING-TYPE: new
 DOCUMENT-IDENTIFIER: US 20020194501 A1

TITLE: System and method for conducting a secure interactive communication session

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 713/201; 713/150

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems,

methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable, deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	In
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☐ 9. Document ID: US 20020194483 A1

L19: Entry 9 of 41

File: PGPB

Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020194483

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020194483 A1

TITLE: System and method for authorization of access to a resource

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 713/185

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems, methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable, deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	In
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☐ 10. Document ID: US 20020178360 A1

L19: Entry 10 of 41

File: PGPB

Nov 28, 2002

PGPUB-DOCUMENT-NUMBER: 20020178360
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020178360 A1

TITLE: System and method for communicating a secure unidirectional response message

PUBLICATION-DATE: November 28, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 713/170

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems, methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable, deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	In
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☐ 11. Document ID: US 20020170050 A1

L19: Entry 11 of 41

File: PGPB

Nov 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020170050
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020170050 A1

TITLE: Methods and apparatus for upgrading firmware in an embedded system

PUBLICATION-DATE: November 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Fiorella, Daniel Charles III	Blue Bell	PA	US	
Gebhardt, Ronald L. JR.	Delran	NJ	US	
McGregor, Marlin F. JR.	Berwyn	PA	US	

US-CL-CURRENT: 717/168

ABSTRACT:

The present invention provides methods and apparatus for upgrading firmware in an embedded system, without impacting the system. More specifically, the present invention enables an embedded system to be upgraded without any system downtime, by providing two application areas in non-volatile programmable read only memory. A processor can boot up and run from either application area. A fixed vector table is provided, which, in cooperation with a software vector table, enables the processor to maintain proper interrupt vector addresses while being able to run from either application area. Upgraded firmware can be loaded into one application area while the system is running from the other application area. Resetting the processor allows the system to run the upgraded version of firmware.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	In
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☐ 12. Document ID: US 20020165912 A1

L19: Entry 12 of 41

File: PGPB

Nov 7, 2002

PGPUB-DOCUMENT-NUMBER: 20020165912

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020165912 A1

TITLE: Secure certificate and system and method for issuing and using same

PUBLICATION-DATE: November 7, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wenocur, Michael L.	Palo Alto	CA	US	
Baldwin, Robert W.	Palo Alto	CA	US	
Illowsky, Daniel H.	Cupertino	CA	US	

US-CL-CURRENT: 709/203

ABSTRACT:

System, method, signal, operating model, and computer program for electronic messaging. Systems and method for providing security for communication of electronic messages, interactive sessions, software downloads, software upgrades, and other content from a source to a receiving device as well as signals used for such communications. Systems, methods, signals, device architectures, data formats, and computer program structures for providing authentication, integrity, confidentiality, non-repudiation, replay protection, and other security properties while minimizing the network bandwidth, computational resources, and manual user interactions required to install, enable,

deploy and utilize these security properties. System, device, method, computer program, and computer program product for searching and selecting data and control elements in message procedural/data sets for automatic and complete portrayal of message to maintain message intent. System, device, method, computer program, and computer program product for adapting content for sensory and physically challenged persons using embedded semantic elements in a procedurally based message file.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	In
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☐ 13. Document ID: US 6536034 B1

L19: Entry 13 of 41

File: USPT

Mar 18, 2003

US-PAT-NO: 6536034

DOCUMENT-IDENTIFIER: US 6536034 B1

TITLE: Method for modifying code sequences and related device

DATE-ISSUED: March 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nassor; Azad	Villepreux			FR

US-CL-CURRENT: 717/110; 710/22, 710/23, 710/24, 710/25, 717/106, 717/120, 717/136

ABSTRACT:

The present invention relates to a process and a device for modifying code sequences written into a first memory (2) of a medium. A central processing unit (1) executes code sequences and the first memory contains a main program comprising at least one code sequence executable by the central processing unit (1). The first memory also comprises a second, programmable nonvolatile memory (3), and a third working memory (4). A branch table TAB_DER contained in the second programmable memory contains at least one field containing reference data for a new code sequence stored in one of the memories. Branching instructions allow a deferred branch from the executed code sequence to the new code sequence written into one of the three memories. Instructions in the new code sequence allow the return to a point of the code sequence executed before the branch.

23 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	In
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☐ 14. Document ID: US 6105119 A

L19: Entry 14 of 41

File: USPT

Aug 15, 2000

US-PAT-NO: 6105119

DOCUMENT-IDENTIFIER: US 6105119 A

TITLE: Data transfer circuitry, DSP wrapper circuitry and improved processor devices, methods and systems

DATE-ISSUED: August 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kerr; Jeffrey L.	Garland	TX		
So; John Ling Wing	Plano	TX		
Magee; Steven R.	Carrollton	TX		

US-CL-CURRENT: 711/219; 710/110

ABSTRACT:

An integrated circuit (1720) includes a dual-port memory (3330.1) having a first memory port (Port A) and a second memory port (Port B), a bus interface block (5010) including bus master (5016) and bus slave circuitry (5018), and a byte-channeling block (5310) coupled between the first memory port (Port A) and the bus interface block (5010) operable to convert non-aligned data addresses into aligned data. Advantageously, this invention includes a single bus master serving all application hardware. This relieves the host of the extra burden of communicating to slave circuits, reducing host I/O MIPS significantly. The digital signal processor with an ASIC wrapper of this invention together provide super-bus-mastering to access the entire memory space in the system, including the entire virtual memory space accessible by the host processor. Other processes, systems, devices and methods are also disclosed.

2 Claims, 159 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 104

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	In
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☐ 15. Document ID: US 6055619 A

L19: Entry 15 of 41

File: USPT

Apr 25, 2000

US-PAT-NO: 6055619

DOCUMENT-IDENTIFIER: US 6055619 A

TITLE: Circuits, system, and methods for processing multiple data streams

DATE-ISSUED: April 25, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
North; Gregory Allen	Austin	TX		
Gephardt; Douglas D.	Austin	TX		
Barnette; James D.	Austin	TX		
Austin; James D.	Austin	TX		
Haban; Scott Thomas	Austin	TX		

David; Thomas Saroshan Austin TX
Kircher; Brian Christopher Round Rock TX

US-CL-CURRENT: 712/36; 704/270, 712/35

ABSTRACT:

An audio information processing subsystem 200 is disclosed which includes a stream processor 100 for simultaneously processing multiple streams of audio data. Processing subsystem 200 also includes a program memory 202 coupled to stream processor 100 for storing instructions for controlling processing system 200 and a data memory 203/204 also coupled to stream processor 100. Additionally, a direct memory access circuitry 208 is provided for controlling direct memory accesses to a selected one of program memory 202 and data memory 203/204.

30 Claims, 144 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 64

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWIC	Draw Desc	In
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☐ 16. Document ID: US 6000025 A

L19: Entry 16 of 41

File: USPT

Dec 7, 1999

US-PAT-NO: 6000025

DOCUMENT-IDENTIFIER: US 6000025 A

TITLE: Method of signal processing by contemporaneous operation of ALU and transfer of data

DATE-ISSUED: December 7, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Caudel; Edward R.	Houston	TX		
Magar; Surendar S.	Houston	TX		

US-CL-CURRENT: 712/32

ABSTRACT:

A system for real-time digital signal processing employs a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the separate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16.times.16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

22 Claims, 31 Drawing figures

Exemplary Claim Number: 1
Number of Drawing Sheets: 26

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWIC	Draw Desc	In
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☐ 17. Document ID: US 5909559 A

L19: Entry 17 of 41

File: USPT

Jun 1, 1999

US-PAT-NO: 5909559

DOCUMENT-IDENTIFIER: US 5909559 A

TITLE: Bus bridge device including data bus of first width for a first processor, memory controller, arbiter circuit and second processor having a different second data width

DATE-ISSUED: June 1, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
So; John Ling Wing	Plano	TX		

US-CL-CURRENT: 710/307

ABSTRACT:

An integrated circuit (2210) provides on a single chip for use with a first processor (106) off-chip, the following combination: first terminals (of 2232) for first processor-related signals and defining a first data width (32-bit), second terminals for external bus-related signals (PCI), third terminals for memory-related signals (of 2258), and a DRAM memory controller (2250) connected to the third terminals. Further on chip is provided an arbiter circuit (2230), a bus bridge circuit (2236) coupled to the DRAM memory controller and to the second terminals, the bus bridge (2236) also coupled to the arbiter (2230), a second processor (2224) having a second data width (16-bit), and a bus interface circuit (2220)- coupling the second data width of the second processor (2224) to the first data width. The bus interface circuit (2220) further has bus master and bus slave circuitry coupled between the second processor (2224) and the arbiter circuit (2230). The bus bridge (2236), the bus interface (2220) and the first terminals and the DRAM memory controller (2250) have datapaths selectively interconnected in response to the arbiter circuit (2230). Other devices, systems and methods are also disclosed.

5 Claims, 159 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 104

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWIC	Draw Desc	In
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☐ 18. Document ID: US 5854907 A

L19: Entry 18 of 41

File: USPT

Dec 29, 1998

US-PAT-NO: 5854907

DOCUMENT-IDENTIFIER: US 5854907 A

TITLE: Microcomputer for digital signal processing having on-chip memory and external memory access

DATE-ISSUED: December 29, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Caudel; Edward R.	Houston	TX		
Magar; Surendar S.	Houston	TX		

US-CL-CURRENT: 710/100

ABSTRACT:

A system for real-time digital signal processing employs a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the separate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16.times.16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

10 Claims, 31 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 26

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	In
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☐ 19. Document ID: US 5826111 A

L19: Entry 19 of 41

File: USPT

Oct 20, 1998

US-PAT-NO: 5826111

DOCUMENT-IDENTIFIER: US 5826111 A

**** See image for Certificate of Correction ****

TITLE: Modem employing digital signal processor

DATE-ISSUED: October 20, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Caudel; Edward R.	Houston	TX		
Magar; Surendar S.	Houston	TX		

US-CL-CURRENT: 710/69

ABSTRACT:

A system for real-time digital signal processing employs a single-chip microcomputer device (10) having separate on-chip program ROM (14) and data RAM (15), with separate address and data paths for program and data. An external program address bus (RA) allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus (D). A bus interchange module (BIM) allows transfer between the separate internal program and data busses (P-Bus and D-Bus) in special circumstances. The internal busses are 16-bit, while the ALU and accumulator (Acc) are 32-bit. A multiplier circuit (M) produces a single state 16.times.16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter (S) with sign extension.

22 Claims, 32 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 27

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	Keywords	Draw Desc	In
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☐ 20. Document ID: US 5812472 A

L19: Entry 20 of 41

File: USPT

Sep 22, 1998

US-PAT-NO: 5812472

DOCUMENT-IDENTIFIER: US 5812472 A

TITLE: Nested loop method of identifying synchronous memories

DATE-ISSUED: September 22, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lawrence; Archer R.	Austin	TX		
Little; Jack C.	Austin	TX		

US-CL-CURRENT: 365/201; 365/230.03, 365/233, 714/718

ABSTRACT:

A nested loop method for use in a memory test system to identify the width, depth, control line configuration, and part type of a synchronous memory, wherein bit patterns are retrieved from tables representative of a plurality of synchronous memories during execution of nested loops, from outer loop to inner loop, in the order of bank loop, RE loop, CE loop, CS loop, DQMB loop, and part type loop, and bits of an entry of a table occurring after a given entry are either a member of a superset or do not intersect bits of previous entries, and bits of an entry preceding the given entry are either a member of a subset or do not intersect bits of the given entry.

6 Claims, 48 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 48

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	In
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Terms	Documents
L18 and (second near2 (location or area or partition or memory))	41

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☐ 1. Document ID: EP 694851 A2

L12: Entry 1 of 10

File: EPAB

Jan 31, 1996

PUB-NO: EP000694851A2

DOCUMENT-IDENTIFIER: EP 694851 A2

TITLE: Low power consumption micro-controller

PUBN-DATE: January 31, 1996

INVENTOR-INFORMATION:

NAME

COUNTRY

HORST, DIEWALD

DE

INT-CL (IPC): G06 F 15/78; G06 F 1/32

EUR-CL (EPC): G06F015/78

ABSTRACT:

CHG DATE=19990617 STATUS=O> A micro-processor or micro-controller of a module design and adapted for low power is described. Each of the modules is addressed and controller by the CPU in the same way. All assembler instructions and all address modes can be applied to each module. Also, all 16 registers of the CPU are identical in character and can be used with each of the seven address modes. One such device is available in a 4K Byte or 8K Byte ROM, EPROM or RAM version (for prototyping). The high precision 12-bit A/D converter (which can be expanded to 14 bits without additional components) is combined with an LDC drive to output measurement results; the FET driver to switch on loads; the 8-bit Timer/Counter; several I/O ports which accept interrupts; and a watchdog which guarantees safe operation during unexpected events. Somewhere up to 16 nested interrupt levels (7 used in the first product) are active during all Processor/Power modes to capture various external events or timer results. A powerful set of only 51 assembler instructions and 76 address modes allow convenient and fast programming. The CPU can be programmed with minimal effort and a small number of code lines and is extremely economical with ROM space (the number of code lines for a task is a measurement of the programming time).

[Full](#)[Title](#)[Citation](#)[Front](#)[Review](#)[Classification](#)[Date](#)[Reference](#)[Claims](#)[KWIC](#)[Draw Desc](#)[In](#)

☐ 2. Document ID: WO 9212478 A1

L12: Entry 2 of 10

File: EPAB

Jul 23, 1992

PUB-NO: WO009212478A1

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1 **Programming of flash with ICT rights and responsibilities**

Keahey, J.A.;

Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000

Pages:711 - 717

[\[Abstract\]](#) [\[PDF Full-Text \(512 KB\)\]](#) IEEE CNF

2 **PC supported motor drive controller**

Drevensek, D.; Urlep, E.; Curkovic, M.;

Industrial Electronics, 1999. ISIE '99. Proceedings of the IEEE International Symposium on , Volume: 2 , 12-16 July 1999

Pages:647 - 650 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(500 KB\)\]](#) IEEE CNF

3 **A new family of real-time wave and tide instruments**

Trageser, J.I.;

OCEANS '95. MTS/IEEE. 'Challenges of Our Changing Global Environment'.

Conference Proceedings. , Volume: 3 , 9-12 Oct. 1995

Pages:1760 - 1768 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(840 KB\)\]](#) IEEE CNF

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1 A password-protected power controller

Bergman, C.A.;

Southern Tier Technical Conference, 1988., Proceedings of the 1988 IEEE , 19 Oct. 1988

Pages:252 - 257

[\[Abstract\]](#) [\[PDF Full-Text \(244 KB\)\]](#) **IEEE CNF**











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
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1. [Product Update: TrueFFS 5.0 for DiskOnChip \(PU0301, Aug. 2001\) \(PDF\)](#)
... Use **partitions** to store backup images or recovery programs ... No Yes Larger **boot** code
area Saves cost and integration effort for additional **Boot ROM / EEPROM**. ...
www.m-sys.com/files/prodUpd_EOL/doc/PU0301_TFFS_5.0.pdf - [View as html](#)
2. [help on idt platform](#)
... eth0: Missing **EEPROM**, this interface may not ... OK] Activating swap **partitions**: [OK] Setting ... 0xA1FB5D00 - 0xA1FFFFC0 (303808) **Boot area** (physical): 0x01F2C000 ...
www.mail-archive.com/bug-fileutils@gnu.org/msg02215.html - 18k - [Cached](#) - [More pages from this site](#)
3. [dBforums - Help can't boot!](#)
... I had to use the cd to **boot** the install >again and when ... the Solaris and choose fdisk
Set the x86boot fdisk **partition** as active Run "**eeeprom** bootpath" It ...
dbforums.com/arch/187/2002/4/359462 - 14k - [Cached](#)
4. [Sun Archive BOOTROM Page](#)
... SunOS (ie, xy, sd, etc) 0x12 Use **EEPROM** specified **boot** ... hex 0x01c Unit number in hex
0x01d **Partition** number in hex Table for 0x019-0x01d: OS **Boot Device**: 0x019 ...
www.sun3arc.org/FAQ/bootrom.phtml - 8k - [Cached](#)
5. [Password Recovery Procedure-Cisco Lightstream ATM Switches - Cisco ...](#)
... set of bootstrap options 7 - Extended help Option> 5 **booting**: drive:0, **partition**:0, kernel ... START AT 0x10020 NP memory size: 32 MB ILACC: **EEPROM** enet addr:8 ...
www.cisco.com/en/US/products/hw/switches/ps1893/products_password_recovery09186a0080094c4e.shtml - 40k - [Cached](#) - [More pages from this site](#)
6. [\[SUMMARY\] Booting from 2nd disk in Ultra 1](#)
... disk you want to have the root **partition** on ... do the various things for you, including modifying the **eeeprom**. ... c,0. **PRODUCT AREA**: Hardware **PRODUCT**: **Boot PROM** SUNOS ...
www.netsys.com/sunmgr/1998-10/msg00011.html - 19k - [Cached](#) - [More pages from this site](#)
7. [CFE version 1.0.34 for 79EB334 \(32bit,SP,LE\) Build Date: Wed Feb ...](#)
... DS21143 Tulip rev 65 at 0x18800000, **EEPROM** not present ... v1.5 INIT: version 2.78 **booting**
eth0: Setting ... MET 2000 [OK] Activating swap **partitions**: [OK] Setting ...
mail.gnu.org/archive/html/bug-fileutils/2003-03/bxt00001.txt - 8k - [Cached](#) - [More pages from this site](#)
8. [EEPROM Replacement with Flash Memory \(PDF\)](#)
... 64-Kbyte Block 64-Kbyte Block Advanced **Boot** Block Architecture ... and code reside in the same **partition**, and the ... method may be attractive for **EEPROM** emulation, it ...

www.intel.com/design/flcomp/applnots/29782802.pdf - [View as html](#) - [More pages from this site](#)

9. [docs.sun.com: man Pages\(1M\): System Administration Commands](#) 
... flags and names can be set using the **eeeprom**(1M) command ... unix
or /platform/hardware-classname/kernel/unix
from the root **partition**. ... a The **boot** program interprets ...
docs.sun.com/db/doc/802-5747-1M/6i9g1e12l?a=view - 38k - [Cached](#) - [More pages from this site](#)
10. [Roger Kill'em - Handling Computer Viruses](#) 
... erases the hard-drive **boot** sector and **partition** table but ... with a compatible BIOS via
an **EEPROM** Programmer ... Prior to **boot** from harddisk, go into the CMOS setup by ...
www.cyber.net.pk/digiman/article/antivirus.htm - 21k - [Cached](#)
11. [Item - Sun BLUEPRINTS: Boot Disk Management: A Guide For The ...](#) 
... Relocating Volume Components. 6. Maintaining a **Boot** Disk With VERITAS Volume
Manager. ... VxVM
Disk Group Configuration. **Partition** Tables. **EEPROM** Parameters. ...
www.everythinglinux.com.au/item/0130621536?toc=1 - 13k - [Cached](#)
12. [Summary of boot-loaders](#) 
... ABLE. **boot**-loader, GPL. ... Stored in ROM/**EEPROM** - loads images from raw **partition**
on IDE disk. Controlled via serial console when downloading. ...
www.aleph1.co.uk/armlinux/docs/ARMbooting/x115.html - 11k - [Cached](#)
13. [mkcfs](#) 
... device, which can be one of dram, sram, flash, **eeeprom** or eprom. ... size 256K
interleave
1 jedec 0x89bd boot_file "/boot/sys/boot.5025a" **partition** type image ...
www.qnx.com/developer/docs/qnx_4.25_docs/qnx4/utills/m/mkcfs.html - 11k - [Cached](#)
14. [boot\(1M\) manual page](#) 
... flags and names can be set using the **eeeprom**(1M) command ... or /platform/hardware-
class-name/kernel/unix
from the root **partition**. ... a The **boot** program interprets ...
[w3.pppl.gov/cgi-bin/man?page=boot\\$ion=1M](http://w3.pppl.gov/cgi-bin/man?page=boot$ion=1M) - 32k - [Cached](#)
15. [UNIX man pages : boot \(1\)](#) 
... These flags and names can be set using the **eeeprom**(1M) com ... or /platform/hardware-
class-
name/kernel/unix from the root **partition**. ... a The **boot** program interprets ...
www.unidata.ucar.edu/cgi-bin/man-cgi?boot+1 - 31k - [Cached](#) - [More pages from this site](#)
16. [Inferno's /Strongarm/SBOOT\(10.8\)](#) 
... Autoboot can also be cleared by using an **EEPROM** programmer to rewrite the
boot monitor to the flash. ... To see the current **partition** table: P. ...
www.vitanuova.com/inferno/man/10/sboot.html - 17k - [Cached](#)
17. [Info Docs Article 14074](#) 
... These flags and names can be set using the **eeeprom** command from the ... from disk by
the
bootblock program which resides in the **boot area** of a disk **partition**. ...
www.ing.iac.es/~cfg/faq/14074.htm - 45k - [Cached](#)
18. [3.3 Disk Label and Bootblock](#) 
... The SunOS 4.1.X **EEPROM** expects to find bootblock code in ... a disk, sectors 1

through
15 of the first **partition**. ... and allows the PROM to locate the **boot** program on ...
wks.uts.ohio-state.edu/sysadm_course/html/sysadm-51.html - 3k - [Cached](#)

19. [port-hp300: Argh. Can't create bootdisk.](#) 
... 0 # milliseconds >drivedata: 0 > >7 **partitions**: ># size offset ... what I see when **booting**
the 425e ... Video >MC68040 Processor >Configuration **EEPROM** >Utility CHIP at ...
mail-index.netbsd.org/port-hp300/1995/07/25/0000.html - 6k - [Cached](#) - [More pages from this site](#)
20. [Knoppix \(Guide to Running Knoppix\).pmd \(PDF\)](#) 
... an electrically erasable programmable read-only memory (**EEPROM**)—is a ... If you click
on any **partition** you can read its ... Use the F2 feature during **boot** cycle to ...
www.linuxforu.com/editorial/feb2003/Guide.pdf

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DOCUMENT-IDENTIFIER: WO 9212478 A1

TITLE: TRANSACTION AUTOMATION SYSTEM INCLUDING NOVEL MEMORY ARCHITECTURE AND MANAGEMENT

PUBN-DATE: July 23, 1992

INVENTOR-INFORMATION:

NAME

COUNTRY

ECKLEY, GORDON PAUL JR

US

INT-CL (IPC): G06F 7/00; G06F 7/22; G06F 11/00; G06F 12/00

EUR-CL (EPC): G06F012/02; G06F015/16, G06F017/60

ABSTRACT:

A transaction system (100) includes a linear memory (101). Memory locations are noncontiguous, allowing expansion of any memory area without hardware or software modification. Upon power-up the system accesses software stored in ROM (101-1). This software includes the operating system. Once the system is operating under control of ROM (101-1) programs, vector tables are created to allow the system to locate those portions of memory containing predefined operations such as commands, subroutines, or data files. System operation is turned over to EEPROM (101-2) software which modifies the information in the vector tables (101-3b). Control is then turned over to an initialization program in a Battery backed up RAM (101-3), to update the vector tables to define additional files for which there are modified versions in RAM (101-3). Application software in RAM (101-3) then executes, and the system utilizes the vectors for locating the most current version of the software stored in ROM (101-1), EEPROM (101-2), or RAM (101-3).

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	C
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☐ 3. Document ID: GB 2227584 A

L12: Entry 3 of 10

File: EPAB

Aug 1, 1990

PUB-NO: GB002227584A

DOCUMENT-IDENTIFIER: GB 2227584 A

TITLE: Computer control data modification system

PUBN-DATE: August 1, 1990

INVENTOR-INFORMATION:

NAME

COUNTRY

BELL, DONALD

LOMAS, CHARLES

INT-CL (IPC): G06F 12/12

EUR-CL (EPC): G06F009/44; G06F009/445, G06F011/36

ABSTRACT:

CHG DATE=19990617 STATUS=O> A data processing system has an erasable programmable read-only memory (EPROM) 22 for holding firmware, and an electrically-erasable programmable

read-only memory (EEPROM) 23 for holding patch information specifying modifications to be made to the firmware. In operation, code is copied from the EPROM into a random-access memory (RAM) 21 and is then patched using the information in the EEPROM. The EEPROM can be accessed by a remote computer, 18, to write new patches into it. The EEPROM has separate areas for holding new and trusted patches. In operation, an attempt is made to modify the code using the new patches. If this is successful, the new patch area becomes the trusted patch area. Otherwise, the system reverts to the existing

trusted patches, if any.



Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	Keywords	Draw Desc	In
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☐ 4. Document ID: NN86102265

L12: Entry 4 of 10

File: TDBD

Oct 1, 1986

TDB-ACC-NO: NN86102265

DISCLOSURE TITLE: IBM Personal Computer-Based Automotive Electronic Diagnostic Character Set

PUBLICATION-DATA:

IBM Technical Disclosure Bulletin, October 1986, US

VOLUME NUMBER: 29

ISSUE NUMBER: 5

PAGE NUMBER: 2265 - 2271

DISCLOSURE TEXT:

- This article describes a method of modifying the character generator read-only memory (ROM) of the color graphics adapter in an IBM personal computer (PC) in order to implement special character symbols used in automotive applications. Once encoded into ROM these special symbols can be accessed in the alphanumeric mode similar to a standard ASCII character. Thus, a typical automotive repair manual page can be edited and displayed on the IBM PC-based automotive terminal using editor programs such as the IBM PC Personal Editor without the need to generate such a screen in the graphics all-points-addressable mode. This has the effect of greatly reducing the amount of storage and time required to generate such a screen. Eight data bytes are required to specify such a symbol in all-points-addressable mode while one byte specifies it in the alphanumeric mode if the symbol is correctly encoded in ROM. The original character set stored in the character generator ROM of the color graphics adapter is shown in Fig. 1. The first 128 characters are standard ASCII characters. The remaining 128 characters are special characters which are useful in a variety of applications, such as foreign language alphabets, scientific and mathematical notations, block diagram generation, etc. Each character in this set is composed of an 8 x 8 cell, as shown in Fig. 2, which illustrates the bit pattern of character "A". The method disclosed herein modifies the last 128 characters of the ROM and implements the special character symbols used in automotive diagnostics applications shown in Fig. 3. Fig. 4 is a block diagram of the IBM PC Color Graphics Adapter used in the automotive terminal. The ROM is a Mostek MK36000-5 8K byte ROM with an access time of 300 ns and a cycle time of 450 ns. Its pin-out diagram is shown in Fig. 5A. The 356-character set takes up 2K bytes of memory, and it resides in the upper 2K of the ROM. The ROM address lines are configured as shown in the table Fig. 5B. RAO-RA2 are the row address lines of the 6845 CRT controller (Fig. 4). These lines determine which of the eight rows of a character is being scanned. MDO-

MD7 are the memory data bits of the display buffer. These bits select one of the 256 characters in the set the ASCII code of which is stored in the display random-access memory (RAM). Consider the letter 'A', for example. Its ASCII code is 41 hex, and its dot pattern is shown in Fig. 2. When the ASCII code stored in the display buffer is accessed by the CRTIC, the outputs MD7-MD0 of the display buffer assume the binary value 01000001, i.e., 41 hex. When scanning the first row of the character 'A' the ROM address assumes the binary value 1101000001000, i.e., 1A08 hex. This location in ROM contains a data value of 30 hex. When the second row is scanned, the ROM address changes to 1A09 hex containing a value of 78 hex. Thus the dot pattern of character 'A' consisting of 8 bytes is stored at ROM address starting at 1A08 hex and ending at 1A0F hex. For the second set of 128 characters to be modified, the hex ROM address starts at 1C00 up to 1FF0. The table in Fig. 6 lists the dot pattern of the special symbols stored at their respective ROM addresses. These special symbols were encoded in an erasable programmable read-only (EPROM) that has the same footprints as the character ROM; i.e., it has the same pin-outs as the Mostek ROM. The EPROM selected is a Motorola MCM68766C30 which also has the same access and cycle time as the Mostek ROM. As an example, the dot pattern of a character symbol is arrived at by drawing the symbol in an 8 x 8 cell (Fig. 7) and revising it until it displays legibly on the screen. The dot pattern is then arrived at by substituting a binary 1 for every marked box in the cell and a 0 for every blank box.

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Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	C
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☐ 5. Document ID: JP 2003002159 A

L12: Entry 5 of 10

File: DWPI

Jan 8, 2003

DERWENT-ACC-NO: 2003-191766

DERWENT-WEEK: 200319

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TITLE: Airbag controller for vehicle, accesses EEPROM storing correction data of impact determination threshold value when ignition switch of vehicle is operated

PRIORITY-DATA: 2001JP-0192159 (June 26, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2003002159 A	January 8, 2003		007	B60R021/32

INT-CL (IPC): B60 R 21/01; B60 R 21/32

ABSTRACTED-PUB-NO: JP2003002159A

BASIC-ABSTRACT:

NOVELTY - An EEPROM storing correction data of impact determination threshold value is accessed when ignition switch of the vehicle is operated. The correction value is stored in a RAM by judging the alteration of impact determination threshold value in a ROM of CPU. A CPU determines the impact for operating the airbag according to the data stored

in the RAM.

USE - For controlling airbag of vehicle.

ADVANTAGE - Alters data on EEPROM easily while eliminating the need for modification of ROM.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart of airbag controller. (Drawing includes non-English language text).

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	C
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☐ 6. Document ID: JP 2002044693 A

L12: Entry 6 of 10

File: DWPI

Feb 8, 2002

DERWENT-ACC-NO: 2002-213265

DERWENT-WEEK: 200227

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TITLE: Controller of electronic switching system boots old version firmware when restoration reset signal is received from CPU during failure condition

PRIORITY-DATA: 2000JP-0222593 (July 24, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<u>JP 2002044693 A</u>	February 8, 2002		007	H04Q003/545

INT-CL (IPC): G06 F 11/00; H04 Q 3/545

ABSTRACTED-PUB-NO: JP2002044693A

BASIC-ABSTRACT:

NOVELTY - A controller maintains the firmware of an old version and corresponding boot program in EEPROM (10) and EPROM (11), when the firmware of new version and its relevant boot program are written in memories. The old version firmware is stored in back-up area of RAM, when the new version firmware is downloaded. When a restoration reset signal is received from a CPU (2) during failure, the old version firmware is booted by the stored program.

USE - For electronic switching system such as digital switching system.

ADVANTAGE - The property and certainty of failure restoration are rapidly improved, when the failure due to the fault of new firmware is generated. The old firmware is quickly reset while updating the new firmware.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the controller of electronic switching system. (Drawing includes non-English language text).

CPU 2

EEPROM 10

EPROM 11

☐ 7. Document ID: GB 2361783 A, WO 200182305 A1, AU 200152359 A

L12: Entry 7 of 10

File: DWPI

Oct 31, 2001

DERWENT-ACC-NO: 2002-283279

DERWENT-WEEK: 200233

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TITLE: Non-volatile memory data updating method e.g. for flash ROM in mobile telephone, involves reading data from sector having more recent valid data and writing data into associated RAM

INVENTOR: APPLETON, I K

PRIORITY-DATA: 2000GB-0010285 (April 27, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<u>GB 2361783 A</u>	October 31, 2001		013	G06F012/16
<u>WO 200182305 A1</u>	November 1, 2001	E	000	G11C016/10
<u>AU 200152359 A</u>	November 7, 2001		000	G11C016/10

INT-CL (IPC): G06 F 12/16; G11 C 16/10; G11 C 16/22

ABSTRACTED-PUB-NO: GB 2361783A

BASIC-ABSTRACT:

NOVELTY - A sector (A) having more recent valid data is selected from the memory and the data is read from the selected sector. The read data is stored in associated RAM and updated. The data in the sector (B) which is not selected, is erased and data from RAM is stored in sector (B).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for computer readable storage medium storing data updating program.

USE - For updating data stored in non-volatile memory such as EEPROM, flash ROM used for mobile telephone and digital TV set-top decoder.

ADVANTAGE - Since data from selected sector is stored in associated RAM, the need for separate EEPROM is eliminated and the loss of data if power supply is interrupted during sector erase phase is prevented.

DESCRIPTION OF DRAWING(S) - The figure shows the flow diagram explaining method of updating data in non-volatile memory.

Sectors A,B

☐ 8. Document ID: CN 1230728 A

DERWENT-ACC-NO: 2000-063332
 DERWENT-WEEK: 200007
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TITLE: Personal data assistant system with changeable system program

INVENTOR: DING, S

PRIORITY-DATA: 1998CN-0105181 (March 27, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
CN 1230728 A	October 6, 1999		001	G06F017/40

INT-CL (IPC): G06 F 3/00; G06 F 13/00; G06 F 17/40

ABSTRACTED-PUB-NO: CN 1230728A
 BASIC-ABSTRACT:

NOVELTY - The personal data assistant system includes: ROM to store updated formula program being unchangeable after stored; EPROM to store the first system program maintaining after power off; RAM to store download program for downloading the second system program to EPROM and personal data; CPU to process external data to obtain updated formula program; and display to display input signal.

USE - For use as a personal data assistant.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	Keywords	Draw Desc	In
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☐ 9. Document ID: EP 601704 A1, DE 69323840 E, US 5623604 A, EP 601704 B1

L12: Entry 9 of 10

File: DWPI

Jun 15, 1994

DERWENT-ACC-NO: 1994-185101
 DERWENT-WEEK: 199921
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TITLE: Remote writing of firmware to PROM on network board with LAN interface - revising or adding files by downloading ROM firmware image from remote LAN device to PROM on interactive board

INVENTOR: BARRETT, L F; KALWITZ, G A ; RUSSELL, W C

PRIORITY-DATA: 1992US-0978411 (November 18, 1992)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 601704 A1	June 15, 1994	E	079	H04L029/06
DE 69323840 E	April 15, 1999		000	H04L029/06
US 5623604 A	April 22, 1997		062	G06F013/38
EP 601704 B1	March 10, 1999	E	000	H04L029/06

INT-CL (IPC): G06F 9/445; G06F 11/22; G06F 13/38; H04L 29/06

ABSTRACTED-PUB-NO: EP 601704A

BASIC-ABSTRACT:

The method for remotely writing programmable firmware into a PROM involves activating a LAN communication program. The program broadcasts an inquiry through the network for the designated interactive network board, to receive its location information, and to establish communication with the board.

A ROM firmware image is downloaded into a RAM on the board. The image is validated and the PROM is controlled to erase memory locations, transfer preservable data from the PROM into the ROM firmware image and to load into the PROM the ROM firmware image from the RAM. The designated board may be re-initialised to execute instructions from the firmware image stored in the PROM.

ADVANTAGE - Allows peripheral e.g. printer, to be intelligent, interactive network member eliminating necessity of dedicating personal computer to manage it.

ABSTRACTED-PUB-NO:

EP 601704B EQUIVALENT-ABSTRACTS:

The method for remotely writing programmable firmware into a PROM involves activating a LAN communication program. The program broadcasts an inquiry through the network for the designated interactive network board, to receive its location information, and to establish communication with the board.

A ROM firmware image is downloaded into a RAM on the board. The image is validated and the PROM is controlled to erase memory locations, transfer preservable data from the PROM into the ROM firmware image and to load into the PROM the ROM firmware image from the RAM. The designated board may be re-initialised to execute instructions from the firmware image stored in the PROM.

ADVANTAGE - Allows peripheral e.g. printer, to be intelligent, interactive network member eliminating necessity of dedicating personal computer to manage it.

US 5623604A

In a local area network, a method for remotely updating an old ROM firmware image stored in a PROM disposed on a designated interactive network board having a local area network interface, said method comprising the steps of:

activating a local area network communication program, said communication program operating (i) to broadcast an inquiry through the local area network for the designated interactive network board, (ii) to receive location information of the designated interactive network board in response to the broadcast inquiry, and (iii) to establish communication with the designated interactive network board via the local area network interface;

downloading, over the local area network interface, a new ROM firmware image into a RAM on the designated interactive network board;

verifying that the new ROM firmware image stored in the RAM is valid prior to loading the new ROM firmware image from the RAM into the PROM;

updating firmware of the PROM, in a case where the new ROM firmware image is valid, by (i) storing a predesignated portion of the old ROM firmware image in the RAM, (ii) erasing predetermined PROM storage locations, and (iii) loading the new ROM firmware image and the predesignated portion of the old ROM firmware image from the RAM into the PROM; and

re-initializing the designated interactive network board, in a case where the new ROM firmware image is valid, using the new ROM firmware image and the predesignated portion of the old ROM firmware image loaded in the PROM.

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	RWC	Draw Desc	C
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☐ 10. Document ID: GB 2227584 A, AU 9048795 A, GB 2227584 B, ZA 9000180 A

L12: Entry 10 of 10

File: DWPI

Aug 1, 1990

DERWENT-ACC-NO: 1990-233528

DERWENT-WEEK: 199031

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TITLE: Computer controlled data processing system - has EPROM for holding firmware and EEPROM for holding patch information for modification to firmware which is controlled by computer

INVENTOR: BELL, D; LOMAS, C

PRIORITY-DATA: 1989GB-0001932 (January 28, 1989), 1989GB-0027269 (December 1, 1989)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<u>GB 2227584 A</u>	August 1, 1990		000	
<u>AU 9048795 A</u>	August 2, 1990		000	
<u>GB 2227584 B</u>	September 2, 1992		000	G06F012/12
<u>ZA 9000180 A</u>	October 31, 1990		000	

INT-CL (IPC): G06F 9/24; G06F 12/12

ABSTRACTED-PUB-NO: GB 2227584A

BASIC-ABSTRACT:

The system has an erasable programmable read-only memory (EPROM) (22) for holding firmware. The system also has an electrically-erasable programmable read-only memory (EEPROM) (23) for holding patch information specifying modifications to be made to the firmware. In operation, code is copied from the EPROM into a random-access memory (RAM) (21) and is then patched using the information in the EEPROM. The EEPROM can be accessed by a remote computer (18) to write new patches into it.

The EEPROM has separate areas for holding new and trusted patches. The code is modified using the new patches. The new patch area then becomes the trusted patch area. Otherwise, the system reverts to the existing trusted patches.

ADVANTAGE - Updates and modified data held in ROM without need for physical replacement of ROM.

ABSTRACTED-PUB-NO:

GB 2227584B EQUIVALENT-ABSTRACTS:

A data processing system comprising:- (a) a data processor (b) a read-only memory for holding control information for the data processor, (c) a read/write random access memory, (d) an electrically erasable programmable read-only memory (EEPROM) for holding

modification information defining modifications to be applied to the control information, (e) means for copying the control information from the read-only memory into the random-access memory, and (f) means for using modification information in the EEPROM to modify the copy of the control information in the random-access memory.

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	C
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Terms	Documents
L11	10

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L1

(717/168 |717/169 |717/170 |717/171 |717/172 |717/173 |717/174 |717/175
|717/176 |717/177 |717/178).ccls.

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<input type="checkbox"/>	L1	(717/168 717/169 717/170 717/171 717/172 717/173 717/174 717/175 717/176 717/177 717/178).ccls.	1230

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